REMARKS/ARGUMENTS

Claims 1-20 are now in the application. No claims have been added, cancelled or amended. Reconsideration and reexamination of the above identified patent application is hereby requested.

The Examiner has rejected Claims 1-4, 7 and 11-18 under 35 U.S.C. §103(a) as being unpatentable over Guo (US 5,619,148) ("Guo") in view of Ewen et al. (US 5,301,196) ("Ewen").

The Applicant submits that the invention as claimed in Claim 1 is neither taught, described, nor suggested in Guo, even in view of Ewen.

Claim 1 calls for in part, "providing a third signal by delaying the first signal for a third amount of time". (emphasis added). In a separate step of the method of Claim 1, the first signal is "[stored]... when the clock signal alternates from the first level to the second level, and [provided]... as a second signal a second amount of time later". Thus, according to the method of Claim 1, a first signal is processed in separate, unrelated steps to produce a second signal and a third signal. For an illustration of this method, please see Applicant's Fig. 3 showing a flip-flop 330 and a delay block 340 each separately receiving a first signal from the storage circuit 310, and processing the first signal in parallel to one another to produce a second signal and a third signal, respectively.

In contrast, Guo discloses in Fig. 5 a D-type flip-flop ("DFF") 510. The examiner has indicated that this is equivalent to "storing the data signal when the clock signal alternates

from the first level to the second level, and providing the stored data signal as a first signal a first amount of time later", as claimed in Applicant's Claim 1. Guo also discloses in Fig. 5 a DFF 530. The examiner has indicated that this is equivalent to "storing the first signal when the clock signal alternates from the first level to the second level, and providing the stored first signal as a second signal a second amount of time later", as claimed in Applicant's Claim 1.

If the Examiner's indications are correct, then the second signal as claimed in Applicant's Claim 1 should be present on the output of the DFF 530 in Fig. 5, leading to the input of the and gate 531 and ultimately to the RS Flip-Flop 561. However, the Examiner states that, "Guo disclose[s]... providing a third signal by delaying the first signal for a third amount of time (Figure 5, #561)". (Office Action, p.2). The Applicant respectfully submits that this conclusion and the statements made regarding the DFF 530 are incompatible. The RS Flip-Flop 561 of Guo receives its input, albeit indirectly, from the output of DFF 530 (a second signal), rather than from the output of DFF 510 (a first signal). While Ewen may disclose a half speed clock recovery and data multiplexer circuit, it does not disclose providing a third signal by delaying the first signal for a third amount of time.

Accordingly, Applicant's Claim 1 calls for in part, "providing a third signal by delaying the first signal for a third amount of time" (emphasis added), and Guo discloses the RS Flip-Flop 561 receiving its input from the output of DFF 530

rather than DFF 510. Therefore, the Applicant submits that Claim 1 is not unpatentable over Guo even in view of Ewen.

Claim 1 also calls in part for, "storing the third signal when the clock signal alternates from the second level to the first level, and providing the stored third signal as a fourth signal a fourth amount of time later". (emphasis added). According to Claim 1, storing the third signal is carried out on the opposite edge of the clock signal than the storing of either the data signal or the first signal. This is best illustrated by Fig. 3 of the present Application, showing an inverter at the clock input of flip-flop 350.

Accordingly, because Applicant's Claim 1 calls for in part, "storing the third signal when the clock signal alternates from the second level to the first level" (emphasis added), and because neither Guo nor Ewen disclose the inversion of the clock signal, or a third signal storage in any form, the Applicant submits for a second time that Claim 1 is not unpatentable over Guo in view of Ewen.

Lastly, Claim 1 calls in part for, "providing a reference signal by taking the exclusive-OR of the second signal and the fourth signal" (emphasis added). While neither Guo nor Ewen explicitly disclose providing such a reference signal, the Examiner indicates that, "It would have been obvious to one of ordinary skill in the art at the time of the invention to form a signal indicating whether the generated clock leads or lags the received data". (Office Action, p.3). However, the Applicant

respectfully submits that it could not have been obvious to take the exclusive-OR of the second signal and the fourth signal according to Claim 1 because neither the second signal (provided according to Claim 1 by storing the first signal rather than the second signal, as disclosed by Guo), nor the fourth signal (provided by storing the third signal when the clock signal alternates from the second level to the first level) are themselves disclosed in either reference. As such, the Applicant submits for a third and final time that Claim 1 is not unpatentable over Guo in view of Ewen.

Claims 2-4 are dependent on Claim 1. As such, Claims 2-4 are believed allowable based upon Claim 1 and for the additional limitations contained therein.

The Applicant submits that the invention as claimed in Claim 7 is neither taught, described, nor suggested in Guo, even in view of Ewen.

Claim 7 calls for in part, "a first delay block configures to generate a third signal by delaying the first signal". (emphasis added). According to Claim 7, the first signal is also stored in "a second storage device configured to generate a second signal by receiving and storing the first signal". For an illustration of the processing of the first signal in separate, unrelated devices to separately produce a second signal and a third signal, please see Applicant's Fig. 3 showing a flip-flop 330 and a delay block 340 each separately receiving a first signal from the storage circuit 310, and processing the

first signal in parallel to one another to produce a second signal and a third signal, respectively.

In contrast, Guo discloses in Fig. 5 a D-type flip-flop ("DFF") 510. The examiner has indicated that this is equivalent to "a first storage device configured to generate a first signal by receiving and storing the received data signal", as claimed in Applicant's Claim 7. Guo also discloses in Fig. 5 a DFF 530. The examiner has indicated that this is equivalent to "a second storage device configured to generate a second signal by receiving and storing the first signal", as claimed in Applicant's Claim 7.

If the Examiner's indications are correct, then the second signal as claimed in Applicant's Claim 7 should be present on the output of the DFF 530 in Fig. 5, leading to the input of the and gate 531 and ultimately to the RS Flip-Flop 561. However, the Examiner states that, "Guo disclose[s]... providing a third signal by delaying the first signal for a third amount of time (Figure 5, #561)". (Office Action, p.2). The Applicant respectfully submits that this conclusion and the statements made regarding the DFF 530 are incompatible. The RS Flip-Flop 561 of Guo receives its input, albeit indirectly, from the output of DFF 530 (a second signal), rather than from the output of DFF 510 (a first signal). While Ewen may disclose a half speed clock recovery and data multiplexer circuit, it does not disclose a first delay block configures to generate a third signal by delaying the first signal.

Accordingly, Applicant's Claim 7 calls for in part, "a first delay block configures to generate a third signal by

delaying the first signal" (emphasis added), and Guo discloses the RS Flip-Flop 561 receiving its input from the output of DFF 530 rather than DFF 510. Therefore, the Applicant submits that Claim 7 is not unpatentable over Guo even in view of Ewen.

Claim 7 also calls in part for, "wherein when the first storage device stores the received data, the second storage device stores the first signal, and the third storage device does not store the third signal, and when the third storage device stores the third signal, the first storage device does not store the received data, and the second storage device does not store the first signal." This may be accomplished in an embodiment of the present invention by providing first and second storage devices triggered on the opposite edges of the clock signal when compared to a third storage device, or in any other appropriate embodiment. This exemplary embodiment is shown in Fig. 3 of the present Application, which depicts an inverter at the clock input of flip-flop 350.

Accordingly, because Applicant's Claim 7 calls for in part, "when the first storage device stores the received data, the second storage device stores the first signal, and the third storage device does not store the third signal" (emphasis added), and because neither Guo nor Ewen disclose any means to accomplish this alternating storage scheme, or for that matter a third signal storage in any form, the Applicant submits for a second time that Claim 7 is not unpatentable over Guo in view of Ewen.

Lastly, Claim 7 calls in part for, "a first logic gate configured to perform an exclusive-OR of the second and fourth signals". While neither Guo nor Ewen explicitly disclose such a logic gate, the Examiner indicates that, "It would have been obvious to one of ordinary skill in the art at the time of the invention to form a signal indicating whether the generated clock leads or lags the received data". (Office Action, p.3). However, the Applicant respectfully submits that it could not have been obvious to take the exclusive-OR of the second signal and the fourth signal according to Claim 7 because neither the second signal (generated according to Claim 7 by storing the first signal rather than the second signal, as disclosed by Guo), nor the fourth signal (generated when the first and second storage devices do not store a signal) are themselves disclosed in the prior art. As such, the Applicant submits for a third and final time that Claim 7 is not unpatentable over Guo in view of Ewen.

The Applicant submits that the invention as claimed in Claim 11 is neither taught, described, nor suggested in Guo, even in view of Ewen.

Claim 11 calls for in part, "a first delay element having an input coupled to the output of the first flip-flop". (emphasis added). The Examiner looks to Guo to provide disclosure of this element, citing "Guo disclose[s]... providing a third signal by delaying the first signal for a third amount of time (Figure 5, #561)". (Office Action, p.2).

However, Guo also discloses in Fig. 5 a D-type flip-flop ("DFF") 510. The examiner has indicated that this is equivalent to "a first flip-flop having a data input coupled to a first data input port, and a clock input coupled to a first clock port", as claimed in Applicant's Claim 11. However, the RS Flip-Flop 561 of Fig. 5 (which examiner claims is analogous to the first delay element), is not coupled to the output of the DFF 510 (which examiner claims in analogous to the first flip-flop), but rather to the output, albeit indirectly, of the DFF 530. While Ewen may disclose a half speed clock recovery and data multiplexer circuit, it does not disclose a first delay element having an input coupled to the output of the first flip-flop.

Accordingly, Applicant's Claim 11 calls for in part, "a first delay element having an input coupled to the output of the first flip-flop", and Guo discloses the RS Flip-Flop 561 receiving its input from the output of DFF 530 rather than DFF 510. Therefore, the Applicant submits that Claim 11 is not unpatentable over Guo even in view of Ewen.

Claim 11 also calls in part for, "a first exclusive-OR gate having a first input coupled to the output of the second flip-flop, and a second input coupled to the output of the third flip-flop". While neither Guo nor Ewen explicitly disclose providing such an exclusive-OR gate, the Examiner indicates that, "It would have been obvious to one of ordinary skill in the art at the time of the invention to form a signal indicating

whether the generated clock leads or lags the received data". (Office Action, p.3).

However, the Applicant respectfully submits that it could not have been obvious to provide and exclusive-OR gate having a first input coupled to the output of the second flip-flop according to Claim 11 because neither the second flip-flop (provided according to Claim 11 coupled to the first flip-flop rather than a delay device, as disclosed by Guo) nor the third flip-flop are themselves disclosed in either reference. As such, the Applicant again submits that Claim 11 is not unpatentable over Guo in view of Ewen.

Claims 12-17 are dependent on Claim 11. As such, Claims 12-17 are believed allowable based upon Claim 11 and for the additional limitations contained therein.

The Applicant submits that the invention as claimed in Claim 18 is neither taught, described, nor suggested in Guo, even in view of Ewen.

Claim 18 calls for in part, "A method of modifying a signal path comprising an output of a first flip-flop coupled to an input of a second flip-flop and the output of the first flip-flop and an output of the second flip-flop coupled to a logic gate". Because the prior art does not disclose the output of a first flip-flop coupled to an input of a second flip-flop and the output of the first flip-flop and an output of the second flip-flop coupled to a logic gate according to the method of Claim 18 calls, the Applicant submits that Claim 18 is not unpatentable over Guo in view of Ewen.

Claim 18 also calls in part for, "inserting a third flip-flop between the first flip-flop and the logic gate". Because the prior art does not disclose this third flip-flop, the Applicant again submits that Claim 18 is not unpatentable over Guo in view of Ewen.

Accordingly, in view of the above amendment and remarks it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,
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